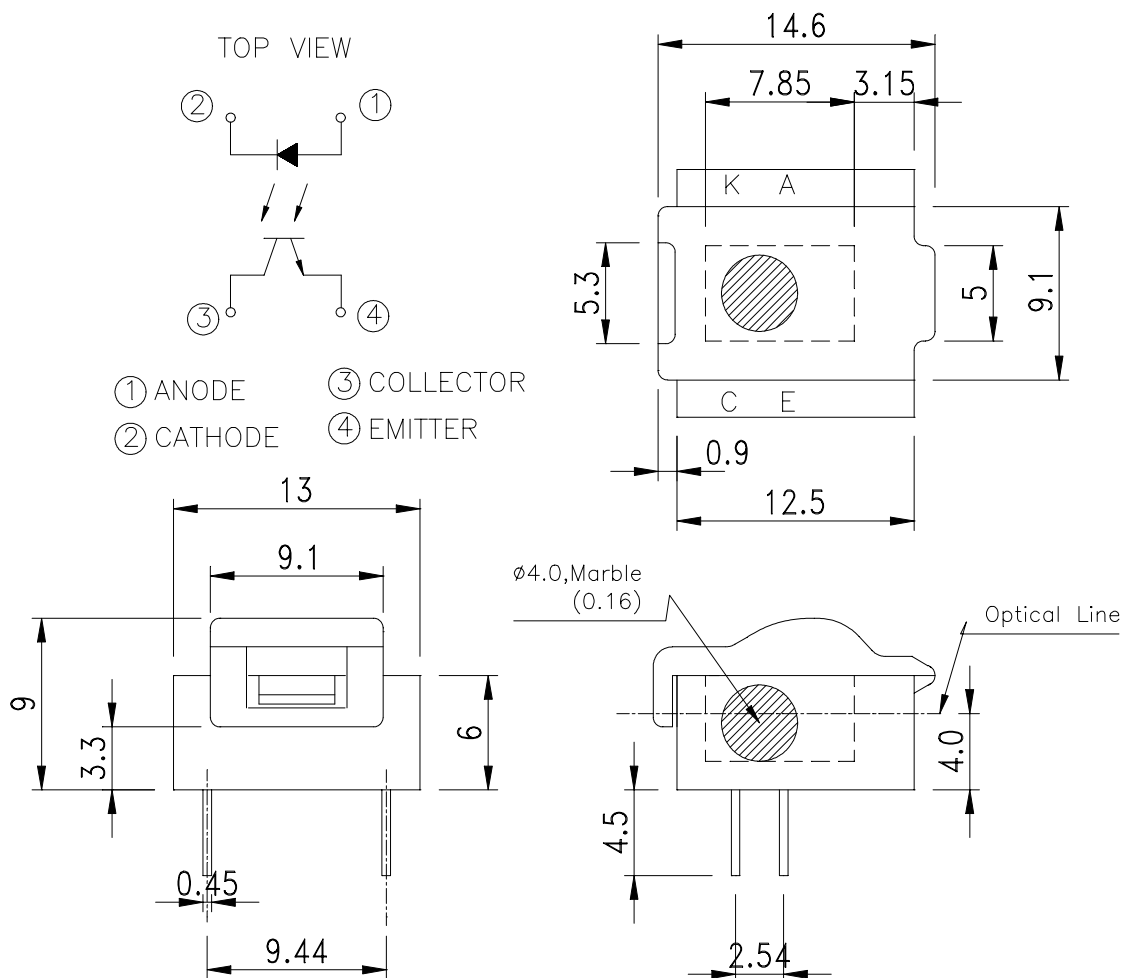


FEATURES

- * NON-CONTACT SWITCHING.
- * FOR DIRECT PC BOARD OR DUAL-IN-LINE SOCKET MOUNTING.
- * FAST SWITCHING SPEED.

PACKAGE DIMENSIONS



NOTES:

1. All dimensions are in millimeters (inches).
2. Tolerance is $\pm 0.25\text{mm} (.010\text{'})$ unless otherwise noted.

ABSOLUTE MAXIMUM RATINGS AT T_A=25

PARAMETER	MAXIMUM RATING	UNIT
INPUT DIODE		
Power Dissipation	75	mA
Peak Forward Current (300 pps , 10 μ S pulse)	1	A
Continuous Forward Current	50	mA
Reverse Voltage	5	V
OUTPUT PHOTOTRANSISTOR		
Power Dissipation	100	mW
Collector-Emitter Voltage	30	V
Emitter-Collector Voltage	5	V
Collector Current	20	mA
Operating Temperature Range	-25 to + 85	
Storage Temperature Range	-55 to + 100	
Lead Soldering Temperature [1.6mm (.063") Form Case]	260 for 5 Seconds	

ELECTRICAL OPTICAL CHARACTERISTICS AT $T_A=25$

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITION
INPUT DIODE							
Forward Voltage		V_F		1.2	1.6	V	$I_F = 20\text{mA}$
Reverse Current		I_R			100	μA	$V_R=5\text{V}$
OUTPUT PHOTOTRANSISTOR							
Collector-Emitter Dark Current		I_{CEO}			100	nA	$V_{CE}=10\text{V}$
COUPLER							
Collector-Emitter Saturation Voltage		$V_{CE(SAT)}$			0.4	V	$I_C=0.5\text{mA}$ $I_F=20\text{mA}$
On State Collector Current		$I_{C(ON)}$	0.5	2		mA	$V_{CE}=5\text{V}$ $I_F=20\text{mA}$
Response Time	Rise Time	T_R		3	15	μS	$V_{CE}=5\text{V}, I_C=2\text{mA}$ $R_L=100$
	Fall Time	T_F		4	20		

TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25 Ambient Temperature Unless Otherwise Noted)

Fig.1 Power Dissipation vs. Ambient Temperature

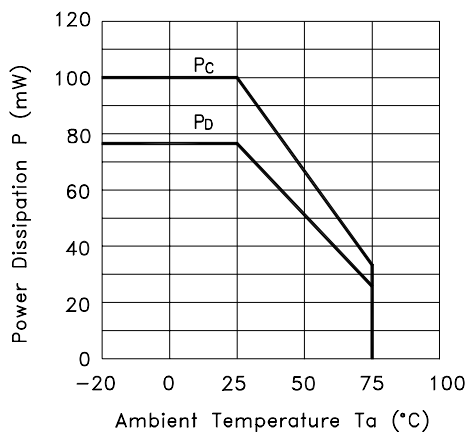


Fig.2 Forward Current vs. Forward Voltage

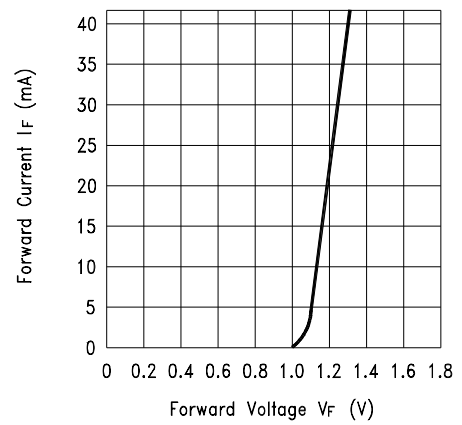


Fig.3 Collector Current vs. Forward Voltage

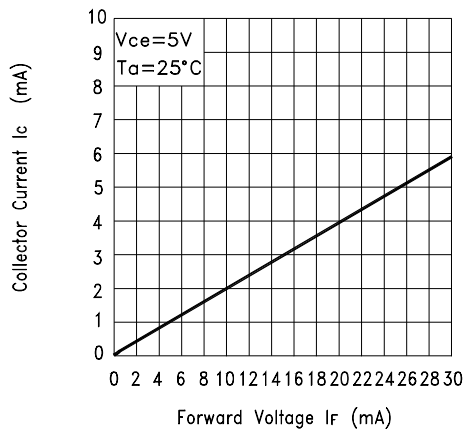
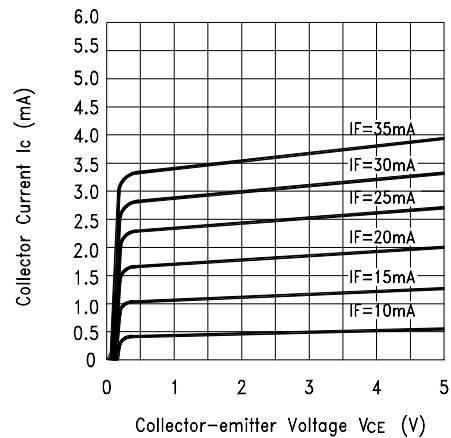


Fig.4 Collector Current vs. Collector-emitter Voltage



TYPICAL ELECTRICAL / OPTICAL CHARACTERISTICS CURVES

(25 Ambient Temperature Unless Otherwise Noted)

Fig.5 Collector Current vs. Ambient Temperature

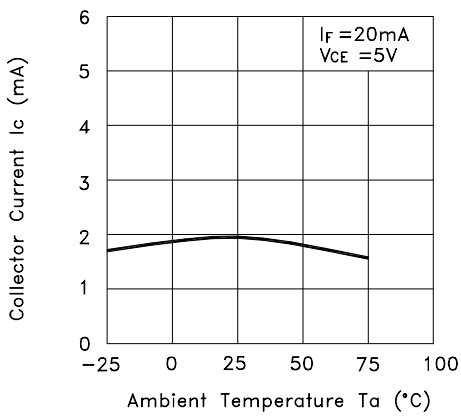


Fig.6 Collector-emitter Saturation Voltage vs. Ambient Temperature

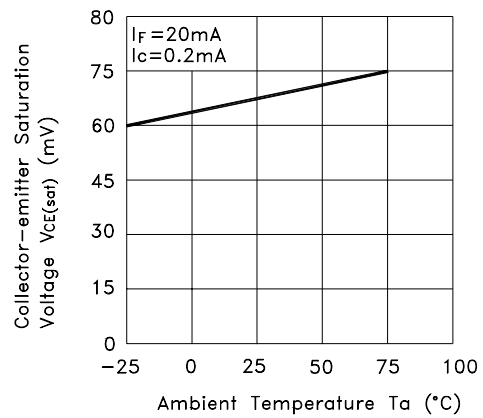
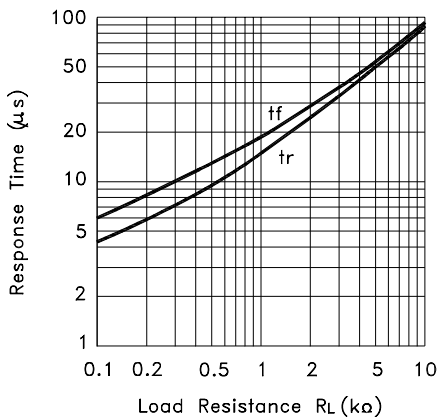


Fig.7 Response Time vs. Load Resistance



Test Circuit for Response Time

